CMOS ANALOG IC DESIGN

QUESTION BANK

M.TECH
(I YEAR – I SEM)
(2023-24)

Department of Electronics and Communication Engineering

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
Recognized under 2(f) and 12 (B) of UGC ACT 1956
(Affiliated to JNTUH, Hyderabad, Approved by AICTE - Accredited by NBA & NAAC – 'A' Grade - ISO 9001:2015 Certified)
Maisammaguda, Dhulapally (Post Via. Kompally), Secunderabad – 500100, Telangana State, India

R22

Code No: R22D6803

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Supplementary Examinations, August 2023

CMOS Analog IC Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 60**

Note: This question paper contains two parts A and B
Part A is compulsory which carries 10 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

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PART-A (10 MARKS)

(Write all answers of this PART at one place)

1	A	Define threshold voltage? Give the expression for it?	**[1M]**
	B	Draw the small signal model for NMOS MOSFET with all considerations	**[1M]**
	C	Draw the circuit diagram for Wilson current mirror?	**[1M]**
	D	What is the value of output resistance when MOSFET is in degeneration?	**[1M]**
	E	What is Current amplifier?	**[1M]**
	F	Draw the single ended differential amplifier circuit diagram?	**[1M]**
	G	List out the op-amp operation parameters.	**[1M]**
	H	Explain about OTA?	**[1M]**
	I	Sketch the transfer characteristic and model for comparator with finite gain?	**[1M]**
	J	Differentiate the Two-stage comparator and Discrete time Comparator	**[1M]**

PART-B(50 MARKS)

SECTION-I

2	***A***	Derive the I-V relationship of the MOSFET in all the possible regions.	**[6M]**
	B	Suggest a region of operation for the same if one wants to design a switch	**[4M]**
		OR	
3	A	Explain about subthreshold conduction?	**[5M]**
	B	Discuss the various short channel effects in MOS devices	**[5M]**

SECTION-II

4	A	Draw and explain about simple current mirror with beat helper.	**[5M]**
	B	Explain about cascode current mirrors.	**[5M]**
		OR	
5	A	Discuss about the charge injection errors in MOS switch.	**[5M]**
	B	Draw the circuit diagram of High swing cascode current mirror circuit?	**[5M]**

SECTION-III

6	A	Derive the voltage gain for telescopic op amp?	**[5M]**
	B	Discuss the principle of current feedback op amp	**[5M]**
		OR	
7	A	Discuss the disadvantages of cascode amplifier under low voltage condition	**[5M]**

		and hence discuss the folded cascode structure to address the same	
	B	Explain the various architectures of high gain amplifiers.	**[5M]**

SECTION-IV

8	A	Explain about PSRS of two stage op amp	**[5M]**
	B	Explain what is meant by dominant pole compensation in operational amplifiers	**[5M]**

OR

9		Explain about single and two stage op amp with neat circuit diagrams	**[10M]**

SECTION-V

10	A	Explain the auto zeroing concept of improving the performance of a comparator.	**[5M]**
	B	Discuss the dynamic characteristics of a Comparator?	**[5M]**

OR

11	A	Give the principle of comparators and characterize the same?	**[5M]**
	B	Explain about Switched capacitor comparators?	**[5M]**

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Code No: R20D6803 **R20**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Supplementary Examinations, August 2023

CMOS Analog IC Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

1	A	Design the Physical structure of an n-channel and a p-channel transistor in a p-well technology.	**[7M]**
	B	Define the threshold voltages in MOS transistor and derive the threshold voltage equation.	**[7M]**
		OR	
2	A	Define latch up and explaintwo prevention methods. What are the advantages of latch up?	**[7M]**
	B	Design the small-signal model for the MOS transistor.	**[7M]**
		SECTION-II	
3	A	Illustrate the hierarchy of analog circuits for the operational amplifier.	**[7M]**
	B	Derive the active resistor equation $r_{ds}$for the MOS diode resistor.	**[7M]**
		OR	
4	A	Design current sinks and source characteristics.	**[7M]**
	B	Draw the I-V characteristics of ideal current and voltage references.	**[7M]**
		SECTION-III	
5	A	Compare Active PMOS load inverter and Current source load inverter.	**[7M]**
	B	Design the noise calculations in a current-source load inverter.	**[7M]**
		OR	
6	A	Design the CMOS differential amplifier using a current-mirror load.	**[7M]**
	B	Calculate the minimum output voltage for the simple Cascode Amplifier.	**[7M]**
		SECTION-IV	
7	A	Design of CMOS Op-Amps and simplified inverting voltage amplifier using an op-amp.	**[7M]**
	B	Give the design procedure for the Two-stage CMOS op-amp.	**[7M]**
		OR	
8		Design the power-supply rejection ratio of two-stage op amps.	**[14M]**
		SECTION-V	
9	A	Design the two-stage, open-loop comparators and its performances.	**[7M]**
	B	Design the clamped push-pull output comparators.	**[7M]**
		OR	
10		Calculate the Propagation delay time of a two-stage open-loop comparator.	**[14M]**

R18

Code No: R18D6808

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Supplementary Examinations, August 2023

CMOS Analog Integrated Circuit Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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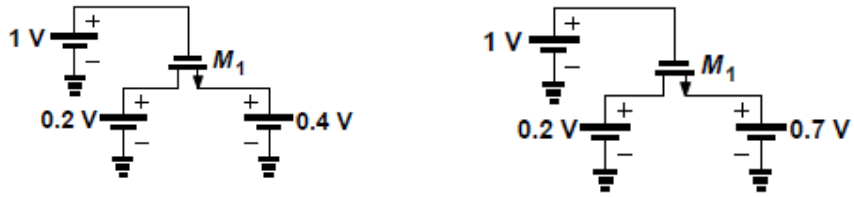
SECTION-I

1	A	Explain the operation of a MOS transistor and derive the mathematical model (drain current equation) in all operating regions	**[7M]**
	B	Determine the operating region and I_D of each of the following MOSFETs. Assume $V_{THn} = 0.4,\ V_{THp} = -0.4, \mu_n C_{0x} = 200\mu A/V^2, \mu_p C_{0x} = 100\mu A/V^2$ W/L=10µm/0.5 µm. lambda=0, gamma=0 	**[7M]**

OR

2	A	What are the different capacitor components compatible with fabrication steps used to build MOS device. Mention the range of values and matching accuracy.	**[7M]**
	B	Draw the small signal model of a MOSFET and derive the small signal parameters	**[7M]**

SECTION-II

3	A	Derive (using small signal analysis) the on-channel resistance of a (i) Diode connected MOSFET in saturation region (ii) MOSFET in linear region	**[7M]**
	B	With neat sketches, compare basic current sink and cascode current sink in terms of voltage overhead and output resistance.	**[7M]**

OR

4	A	Design a basic NMOS current mirror for a output current of 0.75mA from a reference current of 0.5mA and a voltage overhead of 0.3V. Assume $V_{THn} = 0.4,\ \mu_n C_{0x} = 200\mu A/V^2$	**[7M]**
	B	What is an ideal voltage/current reference and mention their performance characteristics? Describe the general principle of a bandgap reference circuit	**[7M]**

SECTION-III

5	A	Draw the circuit diagram of an current source load interver, plot the voltage transfer function and derive its small signal voltage gain	**[7M]**

	B	Give a neat sketch of CMOS differential amplifier with active current mirror load and derive the voltage gain, slew rate and voltage transfer curve	**[7M]**
		OR	
6	A	What are the advantages of cascading?? Provide a circuit implementation of a cascode amplifier (with current mirror biasing) and derive its voltage gain	**[7M]**
	B	Write short notes on high gain amplifier architectures	**[7M]**
		SECTION-IV	
7	A	What is the need for frequency compensation in an opamp? Describe the miller compensation of a two stage op-amp	**[7M]**
	B	Design a two-stage opamp for the below specifications Av=3000V/V, Vdd=2.5V, Vss = -2.5V, GB=10MHz, CL=10pF, SR > 20V/uS, Vout,range=+-2V, ICMR=-1V to 2V, Pdiss=2mW. Assume appropriate material and device parameters	**[7M]**
		OR	
8	A	Provide a neat sketch of nMOS input PMOS cascode folded cascode opamp and derive the output voltage swing, output resistance and small signal voltage gain	**[7M]**
	B	Write short notes on measurement/simulation of gain, bandwidth, CMRR and PSRR of an opamp	**[7M]**
		SECTION-V	
9	A	Describe the model of a comparator with finite gain. Define the static and dynamic characteristics of a comparator	**[7M]**
	B	With a neat sketch, describe the methods to increase the capacitive drive of a tw-stage open loop comparator	**[7M]**
		OR	
10	A	Draw a neat sketch of two-stage open loop comparator and derive its V_{OH}, small signal gain, frequency response and slew rate	**[7M]**
	B	What is the need for comparator with hysteresis? Provide a neat sketch of comparator with hysteresis and plot input/output waveforms with and without hysteresis	**[7M]**

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

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M.Tech I Year I Semester Supplementary Examinations, November 2022

CMOS Analog IC Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Answer Any **Five** Questions

All Questions carries equal marks.

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1	A	Discuss the Passive Components of the MOS transistor?	**[7M]**
	B	Explain sub threshold MOS model?	**[7M]**
2	A	Explain the CMOS device Modelling?	**[7M]**
	B	Draw the small-signal model for the MOS transistor. Briefly explain each component in that?	**[7M]**
3	A	Explain the given simplest forms of the current mirror, the MOS version of the current mirror?	**[7M]**
	B	Explain the Bipolar simple current mirror with degeneration helper with necessary equations?	**[7M]**
4		What is the Current Mirror? Explain the general properties of current mirrors with a block Diagram?	**[14M]**
5	A	Design a CMOS current mirror load differential amplifier?	**[7M]**
	B	Explain the slew rate and noise for a p-channel differential amplifier with necessary equations?	**[7M]**
6	A	Explain about cascade amplifier?	**[7M]**
	B	Explain about the design of CMOS opamps?	**[7M]**
7	A	Explain about the Cascode Op-amps?	**[7M]**

	B	Explain the design of Two-stage op-amps?	**[7M]**
8	A	Compare the dynamic latch with the NMOS and PMOS latches. What are the advantages and disadvantages of the two latches?	**[7M]**
	B	Explain the different types of Open-loop comparator?	**[7M]**

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

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M.Tech I Year I Semester Regular/Supplementary Examinations, June 2022

CMOS Analog IC Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Answer Any **Five** Questions

All Questions carries equal marks.

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1	A	Explain the Large-signal model for the MOS Transistor?	**[7M]**
	B	Explain about computer simulation model?	**[7M]**
2	A	Draw the small-signal model for the MOS transistor. Briefly explain each component in that?	**[7M]**
	B	Choose values of VGS = 1,2,3,4 and 5V, assume that the channel modulation parameter is zero. Sketch to scale the output characteristics of an enhancement n-channel device if VT = 0.7V and ID = 500μA when VGS = 5 Vin saturation.	**[7M]**
3	A	Explain the simplest forms of the current mirror and the Bipolar version of the current mirror?	**[7M]**
	B	Explain in detail the MOS cascode current mirror with necessary equations?	**[7M]**
4	A	Explain the difference between cascade current mirror and Wilson current mirror?	**[7M]**
	B	Write a short notes on current sinks and sources?	**[7M]**

5	A	Briefly explain the differential amplifiers. With necessary equation give the large-signal analysis of CMOS differential amplifiers?	**[7M]**
	B	Derive the expression for power-supply rejection ratio of Two-stage op-amps?	**[7M]**
6	A	Explain about current amplifier?	**[7M]**
	B	Explain the concept of push-pull inverter with a neat diagram. Derive the small signal voltage gain and find the zero in plane?	**[7M]**
7	A	Explain about the design of Two-stage op-amps?	**[7M]**
	B	Explain the compensation of Op-amps?	**[7M]**
8	A	Differentiate the Two-stage comparator and Discrete-time Comparator?	**[7M]**
	B	With neat sketch and necessary equations explain the Design aspect of a two stage open loop comparator for slewing response?	**[7M]**

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Code No: **R18D6808**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Supplementary Examinations, November 2022

CMOS Analog Integrated Circuit Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Answer Any **Five** Questions

All Questions carries equal marks.

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1 Explain about the computer simulation models. **[14M]**

2 Explain the Large-signal model for the MOS Transistor. **[14M]**

3 Discuss about current sinks and sources. **[14M]**

4 Explain the difference between cascade current mirror and Wilson current mirror. **[14M]**

5 Explain about the current amplifier. **[14M]**

6 Explain about the output amplifier. **[14M]**

7 Explain about the design of CMOS op-amps. **[14M]**

8 How to improve the performance of Open loop comparator. **[14M]**

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Code No: **R20D6803**

R20

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Regular Examinations, July 2021

CMOS Analog IC Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Answer Any **Five** Questions

All Questions carries equal marks.

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1 Find the Threshold voltage and Body factor of an n-channel transistor with an n^+ silicon gate if t_{ox} = 200 °A, N_A= 3 X 10^{16} cm^{-3}, gate doping N_D = 4 X 10^{19} cm^{-3}, and if the number of positively charged ions at Gate-Silicon interface per area is 10^{10} cm^{-2}. **[14M]**

2 Interpret the simple MOS large signal model using mathematical models. **[14M]**

3 Model the Voltage reference circuits using voltage division of Resistor and Active device implementation. **[14M]**

4 What is current mirror circuit and discusses its operation using various blocks **[14M]**

5	What is Active load inverter? Develop small signal model for the Active load inverter.	**[14M]**
6	Develop CMOS differential Amplifier and obtain the Differential transconductance of the amplifier.	**[14M]**
7	Draw the block diagram of a general two stage Op-Amp and explain the functionality each block.	**[14M]**
8	Identify model of an Ideal comparator, comparator with finite gain and comparator with input-offset voltage.	**[14M]**

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Code No: R20D6803 **R20**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

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M.Tech I Year I Semester Supplementary Examinati
CMOS Analog IC Design

(VLSI&ES)

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Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

1 Develop the small signal model of MOS transistor and derive the equation for its transconductance. **[14M]**

OR

2 For an n-channel MOSFET with an n^+ silicon gate if t_{ox} = 200 ^oA, N_A= 3 X 10^{15} cm^{-3}, gate doping N_D = 4 X 10^{18} cm^{-3}, and if the number of positively charged ions at Gate-Silicon interface per area is 10^{10} cm^{-2}. Find the V_t and γ of the transistor. **[14M]**

SECTION-II

3 What is Standard Cascode current circuit and discusses its operation using output characteristics. **[14M]**

OR

4	What happens when Gate and Drain of MOS transistor are tied together? Show its I-V characteristics and its small signal model.	**[14M]**

SECTION-III

5	Identify the circuit models for Active load, current source and Push-pull inverters.	**[14M]**

OR

6	Develop CMOS differential Amplifier using current mirror load and obtain the Differential transconductance of the amplifier.	**[14M]**

SECTION-IV

7	List the design procedure parameters of two stage CMOS Op-Amp.	**[14M]**

OR

8	Derive the method for calculating Power-Supply Rejection Ratio and its model.	**[14M]**

SECTION-V

9	Build the circuit model and frequency response of two stage comparator.	**[14M]**

OR

10	Find the propagation delay time of open-loop comparator that has a dominant pole at 10^3 rad/s, DC gain of 10^4, slew rate 1 V/μs, and a binary output voltage swing of 1 V for an applied input voltage 10 mV.	**[14M]**

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Code No: **R18D6808**

R18

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Supplementary Examinations, Decembe

CMOS Analog Integrated Circuit Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

***

SECTION-I

1	a).Discuss about the Passive Components of the MOS transistor.	**[7M]**
	b).Explain about the computer simulation models.	**[7M]**

OR

2	a).Compare NMOS and CMOS technologies with an example.	**[7M]**
	b).Explain sub threshold MOS model.	**[7M]**

SECTION-II

3	a).Write a short note on current sinks and sources.	**[7M]**
	b).Explain the difference between cascade current mirror and Wilson current mirror.	**[7M]**

OR

4	a).Explain in details the MOS cascode current mirror with necessary equations.	**[7M]**
	b).Illustrate the Bipolar version of current mirror with necessary equations.	**[7M]**

SECTION-III

5	a).Explain the concept of push-pull inverter with neat diagram.	**[7M]**

b).Derive the small signal voltage gain and find the zero in plane. **[7M]**

OR

6 a).Name the different output amplifiers and explain any one in detailed. **[7M]**

b).Illustrate the Architectures of High Gain Amplifiers. **[7M]**

SECTION-IV

7 a).Explain about the design of Two-stage op-amps. **[7M]**

b).Demonstrate the Cascode Op-amps. **[7M]**

OR

8 a).Derive the expression for power-supply rejection ratio of Two-stage op-amps. **[7M]**

b).Write a short note on design aspects of Op-Amp. **[7M]**

SECTION-V

9 a).Explain about the different types of Open loop comparator **[7M]**

b).Discuss various types of open loop comparators **[7M]**

OR

10 Elaborate the Performance improvement of Open-Loop Comparators. **[14M]**

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Code No: **R18D6808** **R18**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Supplementary Examinations, February/Mar 2021

CMOS Analog Integrated Circuit Design

(VLSI&ES)

Roll No										

Time: 2 hours 30 min **Max. Marks: 70**

Answer Any **Five** Questions

All Questions carries equal marks.

****

1	a).Draw the small-signal model for the MOS transistor. Briefly explain each component in that.	**[7M]**
	b). Explain about the CMOS device Modelling.	**[7M]**
2	a).Choose values of VGS = 1,2,3,4 and 5V, assume that the channel modulation parameter is zero. Sketch to scale the output characteristics of an enhancement n-channel device if V_T = 0.7V and I_D = 500μA when V_{GS} = 5Vin saturation.	**[7M]**
	b).Explain the Large-signal model for the MOS Transistor.	**[7M]**
3	a).What is Current sink .Explain the general properties of current sink with block diagram?	**[7M]**
	b).Explain in detailed about MOS switch and MOS Diode.	**[7M]**
4	a).Write a short note on MOS switch model.	**[7M]**
	b).Explain about the Bipolar simple current mirror with degeneration helper with necessary equations.	**[7M]**

5	a).Briefly explain the differential amplifiers. With necessary equation give the large signal analysis of CMOS differential amplifiers.	**[7M]**
	b).Design a CMOS current mirror load differential amplifier.	**[7M]**
6	Explain about a) Current Amplifier b) Cascode Amplifier.	**[14M]**
7	With neat sketch explain the following	**[7M]**
	a) Characteristics of Op-Amp b) Classification of Op-Amp	**[7M]**
8	Explain the following terms with neat sketch.	**[7M]**
	a) Switched capacitor comparators b) Regenerative comparators.	**[7M]**

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Code No: **R18D6808**

R18

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year - I Semester Regular/Supplementary Examinations, January-2020

CMOS Analog Integrated Circuit Design

(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

***

SECTION-I

1 Analyze the Simple MOS Small-Signal Model with the associated parameters in detail. **[14M]**

OR

2 a) Illustrate the formation of MOS transistor using n-well technology and threshold voltage. **[7M]**

b) Describe the importance of Sub-threshold MOS Model with relevant diagram **[7M]**

SECTION-II

3 a) Draw the model for a non ideal switch and explain its parameters in detail **[6M]**

b) Draw and explain about a simple current mirror with Beta helper. **[8M]**

OR

4 a) Describe the concept of increasing the output resistance in current sink and the factor by which it is increased? **[7M]**

b) Differentiate between Wilson current mirror and cascode Wilson current mirror **[7M]]**

SECTION-III

5 Illustrate the design of Cascode Amplifiers. **[14M]**

OR

6 Design a CMOS differential amplifier with current mirror load **[14M]**

SECTION-IV

7 a) With a schematic explain about operational-amplifier with its equivalent circuit **[4M]**

b) Define and explain the following terms **[10M]**

i) Common-Mode Input Range

ii) Common-Mode Rejection Ratio

OR

8 a) Briefly explain the Miller compensating networks in op-Amps. **[7M]**

b) Design the two stage CMOS op-amp to meet the important specifications **[7M]**

SECTION-V

9 Describe the following **[7M]**

(a) Auto zeroing technique (b) Comparator using hysteresis **[7M]**

OR

10 a) Discuss the Characterization of Comparator **[7M]**

b) Explain the types of discrete time Comparator. **[7M]**

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Code No: : **R17D6805**

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Supplementary Examinations, Dec-18/Jan-19

CMOS Analog Integrated Circuit Design
(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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			Marks	CO	Blooms Level
		SECTION-I			
Q.1.	a)	Draw the physical structure of n channel and p channel MOS transistor using well technology and highlight the importance points?	**[7M]**	**CO1**	**2**
	b)	Explain the importance of BSIM3 model addresses threshold voltage reduction	**[7M]**	**CO1**	**2**
		OR			
Q.2.	a)	Explain the small signal model for the MOS transistor	**[7M]**	**CO2**	**2**
	b)	Explain about CMOS device model?	**[7M]**		
		SECTION-II			
Q.3.	a)	Explain the the feedback through effects by using a dummy transistor?	**[7M]**	**CO3**	**2**
	b)	Draw the circuit diagram of standard cascode current sink and how its reduces the errors in V or I	**[7M]**		
		OR			
Q.4.	a)	What do you mean by band gap reference and list the principle involved?	**[7M]**	**CO2**	**4**
	b)	Explain 2 Input NOR gate with depletion NMOS loads. Calculate output high voltage and output low voltage?	**[7M]**		
		SECTION-III			
Q.5.	a)	Draw the circuit diagram of output amplifier using push pull inverting amplifier and comment on	**[7M]**	**CO3**	**2**

		it?			
	b)	Explain the noise model of a p channel differential amplifier ?	**[7M]**	**CO3**	**2**
		OR			
Q.6.	a)	Explain the design relationships for the differential amplifier?	**[7M]**	**CO3**	**2**
	b)	Draw the circuit diagram of differential mode and common mode circuits using CMOS and explain?	**[7M]**	**CO3**	**3**

SECTION-IV

Q.7.		What is compensation of Op-amp? Explain the operation of Miller compensation	**[14M]**	**CO4**	**4**
		OR			
Q.8.	a)	Explain the design procedure for the 2 stage CMOS opamp? [7M]	**[7M]**	**CO4**	**3**
	b)	Explain folded cascode op amp? [7M]	**[7M]**		

SECTION-V

Q.9.	a)	Explain regenerative comparators? [7M]	**[7M]**	**CO5**	**4**
	b)	Draw the switched capacitor comparator and highlight four important points	**[7M]**		
		OR			
Q.10.	a)	How to improve the performance of an open loop high gain comparator by auto zeroing?	**[7M]**	**CO5**	**5**
	b)	Explain clamped push pull output comparator	**[7M]**		

Code No: **R18D6808**

R18

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I Year I Semester Supplementary Examinations, October/November 2020

CMOS Analog Integrated Circuit Design

(VLSI&ES)

Roll No										

Time: 2 hours **Max. Marks: 70**

Answer Any **Four** Questions

All Questions carries equal marks.

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1 Write a brief note on various passive components that are available in CMOS technologies with relevant layout diagrams

2 Analyze the Simple MOS Large-Signal Model with the associated parameters in detail.

3 Illustrate the MOS switch operation and various models with application

4 Explain the concept of current sink and Design a current sink of 250µA and a V_{MIN} of 0.5V using self biased high-swing cascade current source.

5 Illustrate the various types of CMOS inverting Amplifiers and small signal model demonstrating the parasitic capacitances

6 a) Design a differential Input Current Amplifier

b) Briefly give a overview of High Gain Amplifiers Architectures

7 Describe the miller compensation of a two stage op amp.

8 Illustrate the discrete-time comparators with relevant schematics

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Code No: R15D6805

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

M.Tech I-Year - I Semester Supplementary Examinations, Dec-18/Jan-19

CMOS Analog Integrated Circuit Design
(VLSI&ES)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 15 marks.

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			Marks	CO	Blooms Level
		SECTION-I			
Q.1.	a)	Explain about MOS large- signal analysis of CMOS Device Modeling	**[10M]**	**CO1**	**2**
	b)	Explain sub-threshold MOS model Parameters.	**[5M]**	**CO1**	**2**
		OR			
Q.2.	a)	Discuss about the passive components of the MOS transistor.	**[7M]**	**CO2**	**2**
	b)	Write about computer simulation models for MOS transistor	**[8M]**	**CO2**	**2**
		SECTION-II			
Q.3.	a)	Explain the working of current mirror with beta helper	**[10M]**	**CO2**	**2**
	b)	Explain the operation of MOS Diode	**[5M]**	**CO2**	**1**
		OR			
Q.4.		Discuss the Cascode current Mirror and Wilson Current Mirror	**[15M]**	**CO2**	**2**

SECTION-III

Q.5.	a)	Explain about working of differential amplifier	**[10M]**	**CO3**	**3**
	b)	Explain the operation of CMOS inverter	**[5M]**	**CO3**	**3**
		OR			
Q.6.		Discuss the principle of High Gain Amplifiers Architectures	**[15M]**	**CO3**	**1**

SECTION-IV

Q.7.		Discuss the concept of op amp compensation and give the necessary expressions.	**[15M]**	**CO4**	**2**
		OR			
Q.8.	a)	Explain the Design of Two-Stage Op Amps	**[10M]**	**CO4**	**6**
	b)	What are the various measurements of op amp?	**[5M]**	**CO4**	**5**

SECTION-V

Q.9.	a)	Explain the Discrete-Time Comparators.	**[7M]**	**CO4**	**2**
	b)	What is a comparator and list the important characteristics of a comparator	**[8M]**	**CO4**	**2**
		OR			
Q.10.		What are the various forms of improving the slew-rate of a 2-stage op amp and obtain the expression for slew rate of CMOS op amp	**[15M]**	**CO5**	**2**